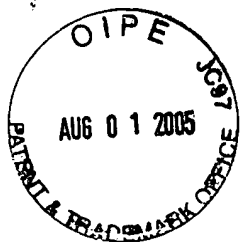
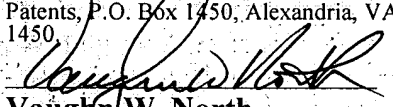


Exhibit 1 Declaration of Applicants



PATENT APPLICATION
ATTORNEY DOCKET NO. 100201669-1

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

<p>ART UNIT: 2891</p> <p>EXAMINER: Christian D. Wilson</p> <p>APPLICANT: Ashton et al.</p> <p>SERIAL NO.: 10/654189</p> <p>FILED: September 3, 2003</p> <p>CONFRM. NO.: 5161</p> <p>FOR: ULTRA-HIGH DENSITY STORAGE DEVICE USING PHASE CHANGE DIODE MEMORY CELLS AND METHODS OF FABRICATION THEREOF</p>	<p>RESPONSE/AMENDMENT</p> <p>CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8</p> <p>DATE OF DEPOSIT: <u>July 27, 05</u></p> <p>I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p> Vaughn W. North</p>
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DECLARATION OF GARY R. ASHTON
UNDER 37 C.F.R. § 1.131

Assistant Commissioner of Patent and Trademarks
Washington, D.C. 20231

I, Gary R. Ashton, declare as follows:

1. I am a named co-inventor in the above-captioned patent application and of the subject matter described and claimed therein.
2. The invention in the above-captioned patent application was conceived and reduced to practice by Gary A. Gibson, Robert N. Bicknell-Tassius and me, collaborating as co-inventors.

3. The invention as described and claimed in the above-captioned US patent application No. 10/654189 was reduced to practice in the United States by Gary A. Gibson, Robert N. Bicknell-Tassius, and me prior to May 1, 2003, the effective date of the Chaiken 499 Published Patent Application.

4. Exhibit 2, attached hereto, is a redacted copy of run logs showing results of the utilization of the claimed invention. Exhibit 2 discloses run log C1462 and run log C1464, both run under my supervision, in collaboration with Gary A. Gibson and Robert N. Bicknell-Tassius. Both run logs C1462 and C1464 show reduction to practice by disclosing samples having In_2Se_3 on a CIGS substrate. The term "CIGS", as disclosed in the above captioned patent application, refers to CuInSe doped with gallium to form various stoichiometric materials of copper indium gallium selenide including but not limited to $(\text{Cu}(\text{In},\text{Ga})\text{Se}_2)$ and $\text{Cu}(\text{In}_{1-x}\text{Ga}_x)\text{Se}_2$. The claimed invention having a substrate containing molybdenum is also disclosed on run log 1464.

5. The documentation attached with the run logs as part of Exhibit 2, namely the EBIC graph for samples C1462 and 1464, shows the EBIC gain as a function of emitter beam voltage for samples C1462 and C1464. The graph describes the samples as having In_2Se_3 as the top layer with CIGS as the bottom layer of three of the four described samples.

6. The attached EBIC graph confirms that the structure of samples C1462 and C1464 includes CIGS as the bottom layer of the diode device. Accordingly, Exhibit 2 shows that the structure described and claimed in the above-captioned patent application was reduced to practice prior to the effective date of May 1, 2003 of the Chaiken 499 Published Patent Application.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statement may jeopardize the validity of the application or any patent issuing thereon.

DATED this 28th day of July, 2005.

Gary R. Ashton
Gary R. Ashton

BEST AVAILABLE COPY

Exhibit 2 to Declaration of Gary R. Ashton



PATENT APPLICATION
ATTORNEY DOCKET NO. 100201669-1

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

<p>ART UNIT: 2891</p> <p>EXAMINER: Christian D. Wilson</p> <p>APPLICANT: Ashton et al.</p> <p>SERIAL NO.: 10/654189</p> <p>FILED: September 3, 2003</p> <p>CONFRM. NO.: 5161</p> <p>FOR: ULTRA-HIGH DENSITY STORAGE DEVICE USING PHASE CHANGE DIODE MEMORY CELLS AND METHODS OF FABRICATION THEREOF</p>	<p>RESPONSE/AMENDMENT</p> <p>CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8</p> <p>DATE OF DEPOSIT: <u>July 29 05</u></p> <p>I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p><u>Vaughn W. North</u> Vaughn W. North</p>
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DECLARATION OF ROBERT N. BICKNELL-TASSIUS
UNDER 37 C.F.R. § 1.131

Assistant Commissioner of Patent and Trademarks
Washington, D.C. 20231

I, Robert N. Bicknell-Tassius, declare as follows:

1. I am a named co-inventor in the above-captioned patent application and of the subject matter described and claimed therein.
2. The invention in the above-captioned patent application was conceived and reduced to practice by Gary R. Ashton, Gary A. Gibson, and me, collaborating as co-inventors.

3. The invention as described and claimed in the above-captioned US patent application No. 10/654189 was reduced to practice in the United States by Gary A. Gibson, Robert N. Bicknell-Tassius, and me prior to May 1, 2003, the effective date of the Chaiken 499 Published Patent Application.

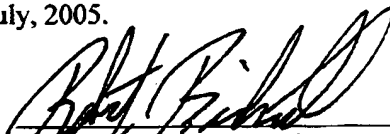
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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statement may jeopardize the validity of the application or any patent issuing thereon.

DATED this 28 day of July, 2005.


Robert N. Bicknell-Tassius

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Exhibit 2 to Declaration of Robert N. Bicknell-Tassius



PATENT APPLICATION
ATTORNEY DOCKET NO. 100201669-1

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

<p>ART UNIT: 2891</p> <p>EXAMINER: Christian D. Wilson</p> <p>APPLICANT: Ashton et al.</p> <p>SERIAL NO.: 10/654189</p> <p>FILED: September 3, 2003</p> <p>CONFRM. NO.: 5161</p> <p>FOR: ULTRA-HIGH DENSITY STORAGE DEVICE USING PHASE CHANGE DIODE MEMORY CELLS AND METHODS OF FABRICATION THEREOF</p>	<p>RESPONSE/AMENDMENT</p> <p>CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8</p> <p>DATE OF DEPOSIT: <u>July 29, 05</u></p> <p>I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p><u>Vaughn W. North</u> Vaughn W. North</p>
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DECLARATION OF GARY A. GIBSON
UNDER 37 C.F.R. § 1.131

Assistant Commissioner of Patent and Trademarks
Washington, D.C. 20231

I, Gary A. Gibson, declare as follows:

1. I am a named co-inventor in the above-captioned patent application and of the subject matter described and claimed therein.
2. The invention in the above-captioned patent application was conceived and reduced to practice by Gary R. Ashton, Robert N. Bicknell-Tassius, and me, collaborating as co-inventors.

3. The invention as described and claimed in the above-captioned US patent application No. 10/654189 was reduced to practice in the United States by Gary A. Gibson, Robert N. Bicknell-Tassius, and me prior to May 1, 2003, the effective date of the Chaiken 499 Published Patent Application.

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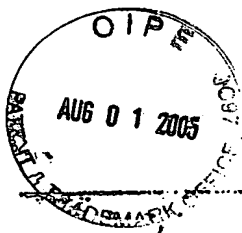
I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statement may jeopardize the validity of the application or any patent issuing thereon.

DATED this 28th day of July, 2005.



Gary A. Gibson

Exhibit 2 to Declaration of Gary A. Gibson



C-System Deposition Log

Run #=	2144	Date=		Operator=	Be
Description:	CLG5 3stage + Inglez				

Calibration							
Parameter	Cu	In-L	In-B	Se	Ga	Zn	Other
PMT RANGE							
PMT CALIB							
Xtal #							
TF							
Pot Setting							
MP							
Cu Xtalk							
Rate A/s @ 3min							
Thk Reading KA							
Thk Measured KA							
Pressure (μ Torr)							

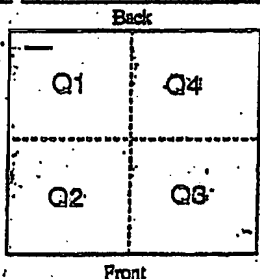
Deposition Parameters							
Base Procedure=	3.1 x 10 ⁻⁶			Emission @ TP2=			
Layer#/Thk	Cu A/s	In A/s	Se A/s		Tm/Ts°C	Dep't	Dep P x10 ⁻⁶
1/							
2/							
3/							
4/							
1Pwr/Amps							
2Pwr/Amps							
3Pwr/Amps							
4Pwr/Amps							

*Includes Xtalk

Comments:

Substrate Mo-SLG

Q1=		Q4=	
Q2=		Q3=	



REST AVAILABLE COPY

C-System Deposition Log

Run # = C1462 Date = Operator = B.B.
 Description: Thylers on various substrates

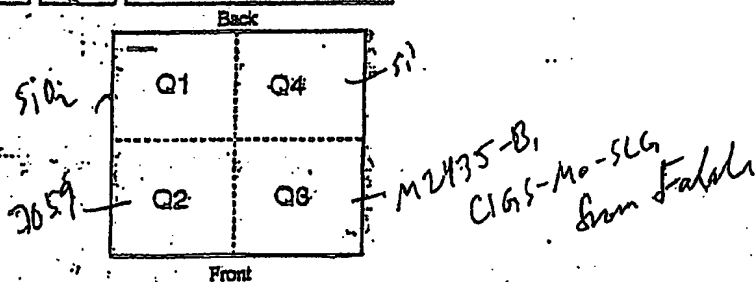
Calibration							
Parameter	Cu	In-L	In-B	Se	As	Zn	Other
PMT RANGE							
PMT CALIB							
Xtal #							
TF							
Pot Setting							
MP							
Cu Xtalk							
Rate A/s @ 3min		4.0		9.5			
Thk Reading KA							
Thk Measured KA							
Pressure (uTorr)							

Deposition Parameters							
Base Pressure	2.6×10^{-6}			Emission @ TP2			
Layer#/Thk	Cu A/s	In A/s	Se A/s		Im/Ts ² C	Dep t	Dep P $\times 10^{-8}$
1/							
2/							
3/							
4/							
1Pwr/Amps							
2Pwr/Amps							
3Pwr/Amps							
4Pwr/Amps							

*Includes Xtalk
 Comments:

Substrate

Q1		Q4	
Q2		Q3	



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